CPU Architecture on an FPGA

Features:

- Custom 16-bit RISC CPU Architecture
  - 12 general purpose registers
  - Special registers: link, status, and stack pointer
  - Arithmetic: add, subtract, multiply, divide, modulo, AND, OR, XOR, NOT, shift logical left, shift logical right
- 12 MHz Clock Speed
- Debugging interface
  - Read register contents to 7-segment displays
  - Clock controls
    - Stop clock
    - Button clock
  - Current Program Count displayed on 7-segment displays
- Memory mapped peripherals
  - LCD
  - 16 GPIO Pins
  - Timers
- Altera DE2 FPGA Development Board