EECE 144
Digital Logic Fundamentals

4 Units: 3 hours of lecture, 2 hours of activity (Engineering Topic)

Course Supervisor/Main Instructor: Dr. Hadil Mustafa/Mr. John-Mark Mamalakis

Required Textbook and Other Course Materials:

Textbook
Digital Design with an Introduction to the Verilog HDL, Sixth Edition, Pearson.

Software and Lab Kit
We are going to use three different software programs this semester. Most of these applications do not always run on a MAC, Linux, Pixelbook, or other tablet type devices, as such a Windows based operating system is suggested so that you can make proper use of the required software for certain assignments. It is your responsibility to have a laptop that meets the standards of the College of Engineering[1]. There are ways to work around this limitation using dual boot or a virtual machine, again this is up to you to set these things up. Links to where the software can be downloaded (for free) will be provided.

Activity sections (lab) will start in the second week of the semester. Before the start of the activity sections you will need to purchase as lab kit (the link to ordering the kit will be provided on-line). This kit is unique to Chico State and contains components for most of the EECE class you will take.

Course Description: Definition and properties of switching algebra. Minimization of algebraic function. Use of Karnaugh maps for simplification. Design of combinational logic networks. Design of sequential logic devices including flip-flops, registers, and counters. Analysis and applications of digital devices. Analysis and design of synchronous and asynchronous sequential state machines, state table derivation and reduction. Use of such CAD tools for schematic capture and logic device simulations. 3 hours lecture, 2 hours activity.

Prerequisites: *GE Mathematics/Quantitative Reasoning Ready.*

Learning Objectives:

Upon completion of this course, students should be able to;

- Apply Boolean Algebra principles to minimize logic functions (SO 1)
- Use Karnaugh Maps and other approaches to minimize Boolean functions (SO 1)
- Design, optimize, and analyze digital circuits (SO 1)
- Design combinational digital components, such as multiplexers, decoders and adders using logic gates (SO 2)
- Design sequential digital circuits using flip-flops and logic gates (SO 2)
- Use hardware description language to design, verify and implement digital circuits at the gate-level of abstraction (SO 2, 7)

[1] https://www.csuchico.edu/ecc/students/prospective/laptop.shtml

Course Topics:

Week	Topic	Reading Assignment
1	Introduction, Number Systems, Number Conversion, Binary Math	1.1-1.4
2	Negative Numbers, 2/s Complement, Coded Numbers, Intro to Binary Logic	1.5-1.7, 1.9
3	Basic Boolean Algebra, Basic Definitions, Theorems and Properties, Boolean Functions	2.1-2.5
4	Minterms and Maxterms, Other Logic Operations, Digital Logic Gates	2.6-2.8
5	Karnaugh Maps, Quiz 1	3.1-3.3
6	Product of Sums, Don't Care, NAND and NOR Implementations, Verilog	3.4-3.7
7	Verilog Intro, Exclusive OR Function, Combinational Circuits	3.8-3..9, 4.1-4.3
8	Analysis of Combinational Circuits Con't, Design Procedure, Verilog Structural Modeling, Exam 1	4.1-4.4
9	Spring Break	
10	Binary Adders	4.5-4.6
11	Decoders and Multiplexrs	4.9, 4.11
12	Sequential Circuits, Latches, Flip-Flops	5.1-5.4
13	State Equations, Analysis, Quiz 2	5.5
14	Mealy and Moore State Machines, Design Procedure	5.6
15	Registers, Shift Registers, Ripple Counters, Synchronous Counters	6.1-6.5
16	Review	

Grading Scheme:

Labs:	25%
Homework:	15%
Quizzes:	20%
Exams:	40%